Amendments to the Specification:

Please replace paragraph [0005] with the following amended paragraph:

This application also relates to application Serial No. ~~09/836,621~~09/839,621, now U.S. Patent No. 6,598,122, entitled "Active Load Address Buffer," filed ~~concurrently herewith~~April 19, 2001, the teachings of which are incorporated by reference herein as if reproduced in full below.

Please replace paragraph [0012] with the following amended paragraph:

One way to protect solid state electronics from faults resulting from cosmic radiation is to surround the potentially effected electronics by a sufficient amount of concrete. It has been calculated that the energy flux of the cosmic radiation can be reduced to acceptable levels with at least six feet of concrete surrounding the chips to be protected. For obvious reasons, protecting electronics from faults caused by cosmic radiation with six feet of concrete usually is not feasible as computers are usually placed in buildings that have already been constructed without this amount of concrete. Because of the relatively low occurrence rate, other techniques for protecting microprocessors from faults created by cosmic radiation have been suggested or implemented that merely check for and correct the transient failures when they occur.

Please replace paragraph [0032] with the following amended paragraph:

The floating point register 122 and integer register 126 are used for the execution of instructions that require the use of such ~~registers as is known by those of ordinary skill in the art~~. These registers 122, 126 can be loaded with data from the data cache 146. The registers also provide their contents to the RUU 130. Figure 2 shows two sets of floating point registers 122 and integer registers 126 for a two-thread processor. However, each thread of the microprocessor preferably has its own set of floating point registers 122 and

integer registers 126, thus multiple sets of these registers may be present, depending on the number of threads of the processor.

Please replace paragraph [0034] with the following amended paragraph:

~~The architecture and components described herein are typical of microprocessors, and particularly pipelined, multithreaded processors.~~ Numerous modifications can be made from that shown in Figure 2. For example, the locations of the RUU 130 and registers 122, 126 can be reversed if desired. For additional information, the following references, all of which are incorporated herein by reference, may be consulted for additional information if needed: U.S. Patent Application Serial No. 08/775,553, now U.S. Patent No. 6,073,159, filed December 31, 1996, and "Exploiting Choice: Instruction Fetch and Issue on an Implementable Simultaneous Multithreaded Processor," by D. Tullsen, S. Eggers, J. Emer, H. Levy, J. Lo and R. Stamm, Proceedings of the 23rd Annual International Symposium on Computer Architecture, Philadelphia, PA, May 1996.